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APPLICATION FOR LETTERS PATENT

BOW RESISTANT PLASTIC SEMICONDUCTOR PACKAGE AND METHOD OF FABRICATION

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Field of the Invention

This invention relates generally to semiconductor packaging and specifically to a method for fabricating plastic semiconductor packages with reduced package bow.

Background of the Invention

A conventional plastic semiconductor package includes a semiconductor die encapsulated in a molded plastic body. The molded plastic body rigidifies and protects the die from the environment. A plastic semiconductor package also includes a metal leadframe wire bonded to bond pads on the die. An adhesive member, such as polyimide tape, or alternately an adhesive layer on the lead frame, attaches the die to the leadframe. The leadframe forms terminal leads for the package and provides internal signal, power and ground paths through the package body to the die.

One aspect of a plastic semiconductor package is that the molded plastic body, the die, the leadframe and the adhesive tape comprise different materials, having different coefficients of thermal expansion (CTE). Because of the different coefficients of thermal expansion, thermo-mechanical stresses are generated within the package as the package is subjected to a temperature change. These stresses are particularly large during manufacture, as the package body cools from a relatively high molding temperature (e.g., 183°C) to room temperature (e.g., 25°C).

One problem that results from these thermo-mechanical stresses is referred to as "package bow" or "package warpage". Figures 1A-1C illustrate different types of package bow, or warpage, in plastic semiconductor packages. In Figure 1A, a semiconductor package 10A includes a plastic body 12A and a plurality of terminal leads 14A extending from

the body 12A on opposed longitudinal sides thereof. The package 10A has undergone a negative bow and has the profile of a "frown". Specifically, the package body 12A has bowed with respect to a theoretical flat profile FP by a warp distance X, which by convention is designated (-). In addition, some of the terminal leads 14A at the center of the package 10A are offset from a theoretical planar reference plane RP by an offset distance of Y.

In Figure 1B, a semiconductor package 10B includes a package body 12B which has undergone a positive bow, and has the profile of a "smile". Specifically, the package body 12B has bowed with respect to the theoretical flat profile FP by the warp distance X, which by convention is designated (+). In addition, some of the terminal leads 14B at the ends of the package 10B are offset from the theoretical planar reference plane RP by the offset distance Y.

In Figure 1C, a semiconductor package 10C includes a package body 12C which has undergone both negative and positive warp distances X, and has an "undulating" profile. In addition, some of the terminal leads 14C in the center of the package 10C, as well as some of the terminal leads 14C at an end of the package 10C, are offset from the theoretical reference plane RP by the offset distance Y.

In each of the packages 10A, 10B, 10C the package bow has been illustrated as occurring along a longitudinal axis of the package. However, package bow can occur along any axis (e.g., lateral axis, diagonal axis) of the package 10A, 10B, 10C. Still further, package bow can be evaluated at any point on the package 10A, 10B, 10C. For example, one method for evaluating package bow is to measure the warp distance X at many different points on a major surface (e.g., top surface or bottom surface) of the package 10A, 10B, 10C. These measurements can be made using a surface laser

profiler, a surface roughness meter, or with other conventional instruments known in the art.

Package bow can also be defined by a "warp factor". SEMI (Semiconductor Equipment and Materials International) defines the warp factor as the warp distance X in mils divided by the length of the package in inches (i.e., WF = X(mils)/L(inches). SEMI standards (SEMI G37-88) for plastic molded small outline packages specify an acceptable warp factor as being 2.5 or less. SEMI standards (SEMI G37-88) also define package warpage as any non-linear dimensional change from the mold cavity characteristic.

One problem resulting from package bow is that the terminal leads 14A, 14B, 14C of the package are no longer co-planar. Without co-planar terminal leads 14A, 14B, 14C, surface mounting of the package 10A, 10B, 10C to a supporting substrate, such as a circuit board, can be difficult. SEMI standards (SEMI G37-88) for plastic molded small outline packages specify that lead co-planarity, measured in a vertical direction, must be within 3 mils (i.e., Y < 3 mils). For making planarity measurements, the reference plane RP can be defined by the three lowest terminal leads 14A, 14B, 14C from the bottom of the package 10A, 10B, 10C. In addition to affecting lead planarity, in lead on chip packages (LOC), package bow can adversely affect the planarity of the leadfingers on the leadframe, and the adhesive bonds to the die.

Also with package bow, once the package is surface mounted to the supporting substrate, additional stresses are generated at the soldered connections between the terminal leads 14A, 14B, 14C and the supporting substrate. These stresses can cause solder joint failure, and can decrease the lifetime of the package 10A, 10B, 10C. Package bow can also cause problems during handling of the packages 10A, 10B, 10C

by automated pick and place equipment, which requires planar surfaces for suction cups to operate properly.

Package bow is particularly troublesome in thin packages, such as thin small outline packages (TSOP). In addition, package bow has become more of a problem due to decreases in the thicknesses of semiconductor dice. Conventional semiconductor dice, for example, have recently decreased in thickness from about 28 mils to about 14 mils. The thinner dice are more likely to bow in a package, and are less likely to provide a rigidifying structure in the package capable of resisting thermo-mechanical stresses.

In view of the foregoing, improved plastic semiconductor packages able to resist bowing, and improved methods for fabricating plastic semiconductor package with reduced bowing, are needed in the art.

Summary of the Invention

In accordance with the present invention, a bow resistant plastic semiconductor package is provided. Also provided are a method for fabricating plastic semiconductor packages with reduced package bow, and improved electronic assemblies fabricated using the plastic semiconductor package.

The plastic semiconductor package includes a die, a lead frame attached to the die, and a plastic body encapsulating the die and the lead frame. In an illustrative embodiment, the package has the configuration of a thin small outline package (TSOP) having terminal leads in a gull wing configuration. Also in the illustrative embodiment, the lead frame and the die have a LOC (lead-on-chip) configuration, and an adhesive member attaches the die to lead fingers on the lead frame. In addition, wire bonds are formed between

bond pads on the die, and the lead fingers on the leadframe, to provide electrical paths therebetween.

The plastic body includes a molded inner member that encapsulates the die, the wire bonds, and portions of the lead fingers proximate to the die. The plastic body also includes a molded outer member, that encapsulates the inner member, and portions of the lead fingers proximate to the terminal leads. The molded inner member provides additional structural strength and rigidity for the package. In addition, the molded inner member is dimensioned to equalize the volume of molding compound in the molded outer member on either side of the leadframe. Stated differently, the molded outer member comprises substantially equal volumes of molding compound on either side of a package parting line.

With the molded outer member comprising substantially equal volumes of molding compound, the magnitude of thermo-mechanical stresses developed as the molding compound undergoes shrinkage during cooling are decreased. The package body is therefore less likely to bow, and cause the terminal leads and the lead fingers to become non-planar. Further, the molded inner member can be at least partially cured prior to molding of the outer member, such that the package body has an internal rigidity for resisting package bow during cooling of the outer member. The molded inner member can also be configured to provide increased structural rigidity for surface mounting the package in electronic assemblies.

The package fabrication method can be performed using a two stage encapsulation process including: a first encapsulation stage for molding the inner member over the die and first portions of the lead fingers, and a second encapsulation stage for molding the outer member over the inner member and second portions of the lead fingers. The two stage encapsulation process can be performed using

separate mold cavities having required geometries, and using the same molding compound for each stage. In addition, the inner member can be at least partially cured prior to molding of the outer member on the inner member.

In an alternate embodiment package, the inner member does not encapsulate the die, but comprises one or more volume equalizing members attached to the lead frame, and encapsulated in the plastic body. The volume equalizing members can comprise an electrically insulating material such as a molding compound, glob top material, or polymer tape. In addition to providing structural strength and rigidity for the package, the volume equalizing members are dimensioned to equalize the volume of molding compound above and below the package parting line.

The bow resistant package improves the construction of electronic assemblies such as printed circuit boards, and multi chip modules. In particular, stresses on bonded connections between the package leads and electrodes on a substrate of the assembly are substantially eliminated due to the planarity of the package leads.

Brief Description of the Drawings

Figure 1A is a schematic side elevation view of a prior art plastic semiconductor package having a negative bow;

Figure 1B is a schematic side elevation view of a prior art plastic semiconductor package having a positive bow;

Figure 1C is a schematic side elevation view of a plastic semiconductor package having multiple bows;

Figure 2A is an enlarged plan view of a plastic semiconductor package constructed in accordance with the invention;

Figure 2B is an enlarged side elevation view of the package;

Figure 2C is an enlarged end elevation view of the package taken along line 2C-2C of Figure 2A;

Figure 2D is an enlarged view of a portion of Figure 2C taken along line 2D of Figure 2C illustrating a terminal lead on the package;

Figure 2E is an enlarged cross sectional view of the package taken along section line 2E-2E of Figure 2A;

Figures 3A-3B are enlarged cross sectional view of the package with parts removed illustrating the molded inner member and the molded outer member of the package body;

Figures 4A-4F are schematic cross sectional views illustrating steps in a method for fabricating the package in accordance with the method of the invention;

Figure 5 is an enlarged cross sectional view, equivalent to Figure 2E of an alternate embodiment semiconductor package having volume equalizing members;

Figure 5A is an enlarged cross sectional view taken along section line 5A-5A of Figure 5 illustrating a volume equalizing member;

Figure 6 is a plan view of an electronic assembly constructed using a plastic package constructed in accordance with the invention; and

Figure 6A is an enlarged cross sectional view taken along section line 6A-6A of Figure 6 illustrating bonded connections between terminal leads of the package and electrodes on a supporting substrate.

Detailed Description of the Preferred Embodiments

Referring to Figures 2A-2E, a plastic semiconductor package 16 constructed in accordance with the invention is illustrated.

In the illustrative embodiment, the package 16 has the configuration of a thin small outline package (TSOP).

However, the package 16 can be fabricated with any other conventional configuration including DIP (dual in line package), ZIP (zig zag in line package), PLCC (plastic leadless carrier), SOP (small outline package), SOJ (small outline j-bend), PQFP (plastic quad flat package), BGA (ball grid array package), PGA (pin grid array package), or LGA (land grid array package).

As shown in Figure 2A, the package 16 includes a generally rectangular shaped plastic body 18 which comprises a molding compound molded into a required shape. The package 16 also includes a plurality of terminal leads 22 projecting from the plastic body 18 along opposed longitudinal edges thereof. As shown in Figure 2D, the terminal leads 22 have a gull wing configuration to permit surface mounting to a supporting substrate, such as a circuit board or a multi chip module substrate. Alternately the terminal leads 22 can have other conventional configurations such as integral standoff, J-bend and butt joint. As also shown in Figure 2A, the package includes notches 24A, 24B along opposed lateral edges of the plastic body 18, and a pin #1 indicator 26 on an upper surface 20 of the plastic body 18.

As shown in Figure 2E, the package 16 also includes a leadframe 28 encapsulated within the plastic body 18 using a molding process to be hereinafter described. In addition, the package 16 includes a semiconductor die 32 attached to the leadframe 28 and encapsulated within the plastic body 18. A package parting line 40 is located at the interface of the upper surface of the leadframe 28 and the plastic body 18. In the illustrative embodiment, the leadframe 28 and the die 32 have a LOC (lead-on-chip) configuration, such that lead fingers 30 of the leadframe 28 attach to the die 32 and form the terminal leads 22 for the package 16. Alternately, the leadframe 28 and the die 32 can have other conventional

configurations. For example, the leadframe 28 can include a mounting paddle (not shown) for supporting the die 32.

Adhesive members 38 attach the face of the die 32 to the underside of the lead fingers 30. The adhesive members 38 can comprise LOC tape (e.g., polyimide tape coated with an adhesive), or can comprise an adhesive layer (e.g., polyimide) applied directly to the lead fingers 30. In addition, wire bonds 34 are formed between the lead fingers 30, and the bond pads 36 on the die 32. The bond pads 36 are in electrical communication with the integrated circuits contained on the die 32. The wire bonds 34 thus form separate electrical paths from the integrated circuits to the terminal leads 22.

As also shown in Figure 2E, the plastic body 18 includes a molded inner member 42 that encapsulates the die 32 and a first portion of the leadframe 28 and the lead fingers 30. The plastic body 18 also includes a molded outer member 44 that encapsulates the inner member 42 and a second portion of the lead frame 28 and the lead fingers 30. The molded inner member 42 provides additional strength and rigidity for the package 16. In addition, the molded inner member 42 is configured to equalize the volume of molding compound contained in the molded outer member 44 above and below the leadframe 28 and the package parting line 40.

Referring to Figures 3A and 3B, further characteristics of the molded inner member 42, and the molded outer member 44 of the plastic body 18 are illustrated. As shown in Figure 3A, the molded inner member 42 includes a lower portion 42A, and an upper portion 42B, separated from one another by the leadframe 28 and the die 32. The lower portion 42A of the molded inner member 42 encapsulates the die 32, and covers a lower portion of the lead fingers 30. The upper portion 42B of the molded inner member 42 encapsulates the wire bonds 34, and covers a face of the die 32. In addition, the upper

portion 42B covers portions of the lead fingers 30 proximate to the die 32. During a molding process to be hereinafter described, a geometry of the molded inner member 42 is selected such that the molded outer member 44 (Figure 3B) will have substantially equal volumes of molding compound above and below the package parting line 40.

As shown in Figure 3B, the molded outer member 44 also includes a lower portion 44A and an upper portion 44B. The lower portion 44A of the molded outer member 44 encapsulates the lower portion 42A of the molded inner member 42, and covers a lower portion of the leadframe 28 proximate to the terminal leads 22 (Figure 2E). The upper portion 44B of the molded outer member 44 encapsulates the upper portion 42B of the molded inner member 42 and covers an upper portion of the leadframe 28 proximate to the terminal leads 22 (Figure 2E). Again the geometry of the molded outer member 44, and of the molded inner member 42, are selected such that the lower portion 44A, and the upper portion 44B of the molded outer member 44 comprise substantially equal volumes of molding compound.

The relationship of the volumes of lower portion 44A and upper portion 44B of the molded outer member 44 can be expressed mathematically as $V_{44A} = V_{44B}$. As is apparent, the relative volumes can be ascertained by consideration of the relevant geometries of the inner member 42, and the outer member 44 including thicknesses and areas. With this configuration for the package body 18, there are substantially equal volumes of molding compound in the molded outer member 44 on either side of the leadframe 28. In addition, there are substantially equal volumes of molding compound in the molded outer member 44 on either side of the package parting line 40. The equal volumes of molding compound help to minimize thermo mechanical stresses during cooling of the molding compound following molding of the

outer member 44. With a reduction in the thermo mechanical stresses package bowing is also significantly reduced. In addition, the planarity of the lead fingers 30 and of the terminal leads 22 is improved.

Referring to Figures 4A-4F, steps in a method for fabricating the semiconductor package 16 are illustrated. Initially, as shown in Figure 4A, the leadframe 28, the adhesive members 38 and the semiconductor die 32 are provided.

Next, as shown in Figure 4B, the die 32 is attached to the lead fingers 30 of the leadframe 28 using the adhesive members 38. The die attach step can be performed using conventional die attach equipment and procedures. As also shown in Figure 4B, the wire bonds 34 are formed between the die bond pads 36 and corresponding connection points on the lead fingers 30. Conventional wire bonding equipment can be used to form the wire bonds 34.

Next, as shown in Figure 4C, a transfer molding press 62 that includes a first mold cavity 50 is provided. The transfer molding press 62 also includes a mold cavity gate 52 in flow communication with the first mold cavity 50, and a runner 54 in flow communication with a source of pressurized molding compound.

Using the transfer molding press 62 and the first mold cavity 50, the inner member 42 can be molded over the leadframe 28 and the die 32. The molding compound for the inner member 42 can comprise a conventional molding compound such as an epoxy resin in a B-stage condition. In addition, conventional parameters can be utilized for the molding process including conventional pressures and temperatures. As shown in Figure 4D, the inner member 42 encapsulates the die 32, and encapsulates lower portions of the lead fingers 30 proximate to the die 32. In addition, the inner member 42

encapsulates the wire bonds 34, and encapsulates upper portions of the lead fingers 30 proximate to the die 32.

The dimensions and the geometry of the first mold cavity 50 can be selected to form the inner member 42 with required dimensions and geometry, substantially as previously described. Specifically, the inner member 42 is formed such that the subsequently formed outer member 44 (Figure 4F) will comprise substantially equal volumes of molding compound either side of the leadframe 28, and on either side of the package parting line 40 (Figure 4F).

Prior to molding the outer member 44, the inner member 42 can be at least partially cured to provide an increased structural rigidity. For example, partial curing can be performed at a temperature of about 120°C-180°C for several minutes or more. In addition, the molding compound used to form the inner member 42 can include fillers selected to provide the outer member with desired mechanical and electrical characteristics such as a relatively fast cure time, and an increased rigidity for strengthening the package body 18.

Next, as shown in Figure 4E, a transfer molding press 64 that includes a second mold cavity 56 is provided. The second mold cavity 56 has dimensions and a geometry selected to form the outer member 44 with desired dimensions and geometrical configuration. The transfer molding press 64 also includes a mold cavity gate 58 in flow communication with the second mold cavity 56, and a runner 60 in flow communication with a source of pressurized molding compound.

Using the transfer molding press 64 and the second mold cavity 56, the outer member 44 can be molded over the leadframe 28 the inner member 42. As with the inner member 42, the outer member 44 can comprise a conventional molding compound such as an epoxy resin in a B-stage condition. In

addition, conventional parameters for the molding process including pressures and temperatures can be utilized.

As shown in Figure 4F, the molded package body 18 includes the molded inner member 42, and the molded outer member 44. A volume of the lower portion 44A of the molded outer member 44 is substantially equal to a volume of the upper portion 44B of the molded outer member 44. During cooling of the molded outer member 44, thermo mechanical stresses are less likely to be generated due to these substantially equal volumes. In addition, a magnitude of the thermal mechanical stresses that do develop is less, such that micro cracks are less likely to occur in the structure of the package body 18. Further, a planarity of the terminal leads 22A can be maintained such that the offset Y (Figure 1A) between any lead 22, and a theoretical reference plane RF (Figure 1A) can be less than about 3 mils (.003 inches = .075 mm). Still further, a package bow X (Figure 1A) measured from a theoretical flat profile FP (Figure 1A) can also be less than about 3 mils (.003 inches = .075 mm).

Referring to Figures 5 and 5A, an alternate embodiment package 16A is illustrated. The package 16A includes a semiconductor die 32 and a leadframe 28A having lead fingers 30A substantially as previously described. The package 16A also includes adhesive members 38A for attaching the die 32 to the lead fingers 30A, and wire bonds 34A formed between the die 32 and the lead fingers 30A. In addition, the package 16A includes a package body 18A, and a plurality of terminal leads 22A extending from the package body 18A.

The package 16A also includes one or more volume equalizing members 66 formed on the leadframe 28A. The volume equalizing members 66 have a volume (length x width x depth) selected to equalize a molding compound volume of a lower portion 18AL of the package body 18A, relative to a molding compound volume of an upper portion 18AU of the

package body 18A. Accordingly, there is a substantially equal volume of molding compound on either side of the leadframe 28A, and substantially equal volumes above and below a parting line 40A of the package 16A. As previously explained, the substantially equal volumes help to minimize thermo mechanical stresses during molding and curing of the package body 18A.

In the illustrative embodiment, the volume equalizing members 66 have a generally rectangular cross section. Alternately, the volume equalizing members 66 can have other cross sections (e.g., circular, oval, triangular). As shown in Figure 5A, the volume equalizing members 66 extend across the lower surfaces of the lead fingers 30A of the leadframe 28A.

The volume equalizing members 66 can comprise molded members formed by a molding compound substantially as previously described for inner member 42 (Figure 2E). In addition, the package body 18A can be formed on the leadframe 28A, die 32 and volume equalizing members 66 using a molding compound and a transfer molding process substantially as previously described for package body 18 (Figure 2E).

Alternately, the volume equalizing members 66 can comprise an electrically-insulating, deposited and cured polymer material such as an epoxy, silicone, room temperature vulcanizing (RTV) or polyimide material. Suitable compounds are commercially available from Dexter-Hysol and from Thermoset. One method for depositing such a polymer material is by dispensing from a nozzle or a needle, in the manner of a "glob top" encapsulant.

As another alternative, the volume equalizing members 66 can comprise a tape material such as a polyimide tape coated on one or both sides with a thermosetting or thermoplastic adhesive. Such a tape can be a commercial tape similar to

die attach tape manufactured by Sumitomo Metal & Mining, and Hitachi Chemical Co., Ltd.

Referring to Figures 6 and 6A, an electronic assembly 68 fabricated using semiconductor packages 16 or 16A, constructed in accordance with the invention is illustrated. The electronic assembly 68 can be configured as a printed circuit board, a multi chip module, or a sub assembly of electronic product such as a field emission display. The electronic assembly includes a supporting substrate 70 and a plurality of packages 16 or 16A, surface mounted to the supporting substrate 70. Depending on the application, the supporting substrate 70 can comprise a ceramic, plastic or printed circuit board material (e.g., FR-4).

The terminal leads 22 or 22A, of the package 16 or 16A, are bonded to corresponding electrodes 72 (Figure 6A) on the supporting substrate 70, using a suitable bonding process such as soldering, or curing of a conductive polymer. Because the terminal leads 22 or 22A are substantially co-planar, stress loads between the terminal leads 22 or 22A, and the electrodes 72 are substantially reduced. In addition, an offset Z between the lower surface 74 of the package 16 or 16A, and the supporting substrate 70 can be accurately maintained without generating stress loads.

Thus the invention provides an improved bow resistant plastic semiconductor package, and a method for fabricating plastic semiconductor packages with reduced package bow. In addition, the package can be used to fabricate improved electronic assemblies such as multi chip modules without stressing bonded connections to a supporting substrate.

While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.